AMENDMENTS TO THE CLAIMS:

Please amend the claims as follows, substituting any amended claim(s) for the corresponding pending claim(s):

1. (Withdrawn) A method of forming a conductive structure within an integrated circuit comprising:

forming a conformal tungsten layer over a dielectric layer and within and filling any unfilled portions of openings within the dielectric layer;

forming an etch protective barrier layer over the tungsten layer, wherein the protective barrier layer comprises a material for which removal by chemical mechanical polishing is primarily mechanical; and

removing at least portions of the etch protective barrier layer and the tungsten layer by chemical mechanical polishing.

2. (Withdrawn) The method as set forth in Claim 1 wherein the step of forming an etch protective barrier layer over the tungsten layer further comprises:

forming a titanium or titanium nitride layer on the tungsten layer.

3. (Withdrawn) The method as set forth in Claim 2 wherein the step of removing at least portions of the etch protective barrier layer and the tungsten layer by chemical mechanical polishing further comprises:

removing portions of the tungsten layer overlying the dielectric layer without removing portions of the tungsten layer within the openings within the dielectric layer.

4. (Withdrawn) The method as set forth in Claim 3 wherein the step of removing at least portions of the etch protective barrier layer and the tungsten layer by chemical mechanical polishing further comprises:

removing all of the protective barrier layer.

5. (Withdrawn) The method as set forth in Claim 3 wherein the step of removing at least portions of the etch protective barrier layer and the tungsten layer by chemical mechanical polishing further comprises:

removing portions of the etch protective barrier layer overlying dielectric regions between the openings within the dielectric layer.

6. (Withdrawn) The method as set forth in Claim 5 wherein the step of removing at least portions of the etch protective barrier layer and the tungsten layer by chemical mechanical polishing further comprises:

after removing portions of the etch protective barrier layer overlying the dielectric regions between the openings within the dielectric layer, removing portions of the tungsten layer overlying the dielectric regions between the openings within the dielectric layer; and

during removal of portions of the tungsten layer overlying the dielectric regions between the openings within the dielectric layer, removing portions of the etch protective barrier layer overlying the openings within the dielectric layer.

7. (Withdrawn) The method as set forth in Claim 2 wherein the step of removing at least portions of the etch protective barrier layer and the tungsten layer by chemical mechanical polishing further comprises:

removing portions of the etch protective barrier layer and the tungsten layer overlying dielectric regions between the openings within the dielectric layer to planarize remaining portions of the tungsten layer and remaining portions of the etch protective barrier layer, if any, with the dielectric layer.

8. (Previously Presented) A portion of an integrated circuit structure comprising:

a dielectric layer over a substrate;

a conformal tungsten layer over the dielectric layer and within and filling any unfilled portions of openings within the dielectric layer; and

an etch protective barrier layer overlying portions of the tungsten layer within the openings but not overlying portions of the tungsten layer over the dielectric layer, wherein the etch protective barrier layer comprises a material for which removal by chemical mechanical polishing is primarily mechanical.

9. (Previously Presented) The portion of an integrated circuit structure as set forth in Claim 8 wherein the etch protective barrier layer is titanium or titanium nitride.

10. (Original) The portion of an integrated circuit structure as set forth in Claim 8 wherein portions of the tungsten layer within the openings are thicker than portions of the tungsten layer over the dielectric layer.

11. (Previously Presented) The portion of an integrated circuit structure as set forth in Claim 8 wherein the etch protective barrier layer overlies the entire tungsten layer.

12. (Cancelled).

13. (Original) The portion of an integrated circuit structure as set forth in Claim 8 wherein the tungsten layer has a thickness of between about 4500 and 8000 angstroms.

14. (Previously Presented) The portion of an integrated circuit structure as set forth in Claim 8 wherein the etch protective barrier layer has a thickness of between about 100 and 800 angstroms.

15. (Original) The portion of an integrated circuit structure as set forth in Claim 8 wherein at least one opening within the dielectric layer is sized to form a capacitive electrode from tungsten within the at least one opening.

16. (Currently Amended) A portion of an integrated circuit structure comprising:

a dielectric layer having an opening therein;

tungsten within the opening and filling a majority of a depth of the opening across a width of the opening, an upper surface of the tungsten within a central region of the opening below an upper surface of the dielectric layer; and

a portion of an etch protective barrier layer over only a central region of the tungsten and within the opening, but not over either peripheral regions of the tungsten within the opening or portions of the tungsten layer over the dielectric layer, wherein the portion of the etch protective barrier layer comprises a material for which removal by chemical mechanical polishing is primarily mechanical.

17. (Previously Presented) The portion of an integrated circuit structure as set forth in Claim 16 wherein an upper surface of the tungsten is exposed around the portion of the etch protective barrier layer.

18. (Previously Presented) The portion of an integrated circuit structure as set forth in Claim 16 wherein the portion of the etch protective barrier layer is titanium or titanium nitride.

19. (Previously Presented) The portion of an integrated circuit structure as set forth in Claim 16 wherein the tungsten outside the central region of the opening and the portion of the etch protective barrier layer form an upper surface which is substantially planar with an upper surface of the dielectric layer.

20. (Original) The portion of an integrated circuit structure as set forth in Claim 16 wherein the opening within the dielectric layer is sized to form a capacitive electrode from the tungsten within the opening.